

Notice of Allowability

Application No.

10/626,242

Examiner

Ishwar (I. B.) Patel

Applicant(s)

ZOLLO ET AL.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on June 10, 2005 and interview summary.
2. ☒ The allowed claim(s) is/are 15,16,18, 19, 20, 22, 23 and 25-34.
3. ☒ The drawings filed on 10 June 2005 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date 7/23/2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413),
Paper No./Mail Date 0605.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Larry G. Brown (Reg. 45,834) on June 20, 2005.

The application has been amended as follows:

(a) In claim 1: Delete "each of", line 5.

(b) Add new claims as below:

25. (New) A method of forming a multilayer circuit board having inverted microvias, comprising the steps of:

providing at least a first substrate core and a second substrate core each of said first substrate core and said second substrate core having a top conductive layer on at least a top side;

forming a microvia on a bottom side of at least one among the first substrate core and the second substrate core, wherein the microvia would reach to the top conductive layer on at least the top side of at least one among the first substrate core and the second substrate core;

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applying a conductive layer to the microvia to interconnect a bottom conductive layer of at least one among the first substrate core and the second substrate core to the top conductive layer of at least one among the first substrate core and the second substrate core;

patterning at least one among the top conductive layer and the bottom conductive layer of at least one among the first substrate core and the second substrate core;

applying an adhesive/bonding layer between at least the first substrate core and the second substrate core;

forming a hole through the first substrate core, the adhesive/bonding layer and the second substrate core;

applying a conductive layer to the hole to interconnect at least two among the top conductive layer of the first substrate core, the top conductive layer of the second substrate core, the bottom conductive layer of the first substrate core, and the bottom conductive layer of the second substrate core,

applying an external dielectric layer to at least one among the top conductive layer of the first substrate core and the top conductive layer of the second substrate core,

applying an external conductive layer to the external dielectric layer,

creating a microvia through at least one among the external dielectric layer and the external conductive layer to expose at least one among the top conductive layer of the first substrate core and the top conductive layer of the second substrate core, and

applying a conductive layer to the microvia to interconnect the external conductive layer to at least one among the top conductive layer of the first substrate core and the second substrate core.

26. (New) The method of claim 25, wherein the step of forming the microvia comprises forming the microvia on the bottom side of the first substrate core and forming a separate microvia on the bottom side of the second substrate core such that each microvia reaches the respective top conductive layer on the first substrate core and the second substrate core.

27. (New) The method of claim 25, wherein the step of patterning comprises patterning the top conductive layer and the bottom conductive layer of the first substrate core and patterning the top conductive layer and the bottom conductive layer of the second substrate core.

28. (New) The method of claim 25, wherein the step of applying the adhesive/bonding layer comprises applying a dielectric layer between the bottom layers of the first substrate core and the second substrate core.

29. (New) The method of claim 25, wherein the step of applying the adhesive/bonding layer comprises applying a dielectric layer on at least exposed portions of the first substrate core and the second substrate core and on at least portions of the bottom

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conductive layer of the first substrate core and the bottom conductive layer of the second substrate core.

30. (New) The method of claim 25, wherein the step of forming the microvia comprises the step of at least one among plasma etching, chemical etching, YAG laser drilling, CO.sub.2 laser drilling, and photo imaging.

31. (New) the method of claim 25, wherein the step of patterning comprises at least one among the steps of plating, applying photolithography, and etching.

32. (New) The method of claim 25, wherein the method further comprises the step of laminating the first substrate core with the second substrate core by curing the adhesive/bonding layer in a vacuum lamination press.

33. (New) The method of claim 25, wherein the method further comprises forming a hole through the external conductive layer, the external dielectric layer, as well as the first substrate core, the adhesive/bonding layer and the second substrate core and applying a conductive layer to the hole to interconnect at least two among the external conductive layer, the top conductive layer of the first substrate core, the top conductive layer of the second substrate core, the bottom conductive layer of the first substrate core, and the bottom conductive layer of the second substrate core.

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34. (New) The method of claim 33, wherein the step of patterning comprises at least one among the steps of plating, applying photolithography, and etching.

2. The following is an examiner's statement of reasons for allowance:

Regarding claims 15, 16, 18 and 19:

A multilayer circuit board with the limitation "(w)herein the conductive layer of the microvia of the external dielectric layer contacts the conductive layer of the first substrate core or the second substrate core and wherein the microvia are vertically aligned with one another" in conjunction with other claimed limitations has not been disclosed by the prior art of record, alone or in combination.

Regarding claims 20, 22 and 23:

A multilayer circuit board with the limitation "(w)herein the conductive interconnection of the first microvia contacts the conductive interconnection of the second microvia and wherein the first and second microvias are vertically aligned with one other" in conjunction with other claimed limitations has not been disclosed by the prior art of record, alone or in combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Claims 1-14 were withdrawn from consideration as a result of restriction requirement. Nevertheless, claims 9-12 contained the subject matter indicated as allowable with respect to product claim 15. As such method claims (after amending claim 1 with the subject matter of claims 9-12), are being rejoined and allowed. Nevertheless, these method claims were cancelled; the method claims, which commensurate with scope of allowable product claim, have been rejoined as claims 25-34.

Note: Information Disclosure Statement (non patent literature) filed on July 23, 2003, considered in the previous action, is withdrawn as date for the document could not be established. See applicant's response filed on June 10, 2005, page 11, line 9-13.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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June 20, 2005



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